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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HARKNESS, CHARLES A	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/580,755	WANG ET AL.	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-9,11 and 31-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-9,11 and 31-54* is/are rejected.

7)☒ Claim(s) *34 and 52* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. There are several grammatical mistakes in the claims including: claim 34 recites "first and second memories are is"; claim 52 recites "where the memory sores"; and the discrepancy in the claims on how non-essential code is spelled, or hyphenated. The applicant or their representatives are urged to review the claims and submit corrections for all mistakes of a grammatical, clerical, or typographical nature. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims rejected under 35 U.S.C. 102(b) as being anticipated by Asghar et al., U.S. Patent Number 5,794,068 (herein referred to as Asghar).

2. Referring to claim 1 Asghar has taught a processor comprising a first pipeline configured to execute essential code (Asghar figure 1, numbers 102, 212, 214, abstract, column 4 lines 11-67);

a second pipeline configured to execute non-essential code (Asghar figure 1, abstract column 4 lines 11-67; the code being executed by the DSP is not essential, and could be left unexecuted, and could just allow the CPU to execute as normal, but the code pattern is recognized and then executed optimally by the DSP portion of the processor); and

a conjugate mapping table configured with a plurality of triggers to specify respectively different sequences of the non-essential code to be executed by the second pipeline (Asghar figures 8 and 10, abstract, column 3 line 61-column 4 line 11); and

a microarchitecture structure coupled to both the first and second pipelines to process code from the first pipeline, and to process code from the second pipeline in response to the triggers (Asghar figure 1, numbers 102, 212, 214, abstract, column 4 lines 11-67).

3. Referring to claim 2 Asghar has taught wherein the first pipeline is coupled to a first instruction cache configured to cache instructions that determine the logical correctness of a program (Asghar figures 2 and 4, number 202, abstract, column 4 lines 11-67).

4. Referring to claim 3 Asghar has taught wherein the second pipeline is coupled to a second instruction cache configured to cache instructions that provide hints for the execution of the instructions that determine the logical correctness of the program (Asghar figure 4, number 444, abstract, column 10 lines 45-64; the data cache holds the operands for the DSP functions and the results).

5. Referring to claim 4 Asghar has taught wherein the first pipeline is coupled to registers that store a micro architectural state, and wherein the conjugate mapping table is responsive to the microarchitectural state (Asghar figure 4, number 454, abstract, column 3 line 61-column 4 line 67).

6. Referring to claim 5 Asghar has taught further comprising:

a first instruction cache coupled to the first pipeline (Asghar figures 2 and 4, number 202, abstract, column 4 lines 11-67); and

a second instruction cache coupled between the conjugate mapping table and the second pipeline (Asghar figure 4, number 444, abstract, column 10 lines 45-64; the data cache holds the operands for the DSP functions and the results).

7. Referring to claim 7 Asghar has taught wherein the conjugate mapping table comprises a plurality of records, each of the plurality of records being configured to map a trigger to a non-essential code sequence (Asghar figures 8 and 10, abstract, column 3 line 61-column 4 line 11).

8. Referring to claim 8 Asghar has taught wherein the trigger comprises an atomic value, such that the conjugate mapping table is configured to specify the non-essential code sequence when the atomic value is satisfied (Asghar figures 8 and 10, abstract, column 3 line 61-column 4 line 11).

9. Referring to claim 9 Asghar has taught wherein the trigger comprises a vector value, such that the conjugate mapping table is configured to specify the non-essential code sequence when the vector value is satisfied (Asghar figures 8 and 10, abstract, column 3 line 61-column 4 line 11).

10. Referring to claim 11 Asghar has taught wherein the microarchitectural structure includes a register bank (Asghar figure 4, number 454, abstract, column 3 line 61-column 4 line 67).

11. Referring to claim 31 has taught further comprising a dynamic code analyzer to generate non-essential code from the essential code in the first pipeline (Asghar figures 8 and 10, abstract, column 3 line 61-column 4 line 67).

12. Referring to claim 32 has taught where the dynamic code analyzer creates directed acyclic graph trace representations of at least some of the essential code from the first pipeline (Asghar figures 8 and 10, abstract, column 3 line 61-column 4 line 67).

13. Referring to claim 33 Asghar has taught a method comprising:

Loading a first instruction stream containing essential code into a first memory (Asghar figures 1 and 4, numbers 202, 102, 212, 214, abstract, column 4 lines 11-67);

Loading a second instruction stream containing non-essential code into a separate second memory (Asghar figure 4, number 444, abstract, column 10 lines 45-64; the data cache holds the operands for the DSP functions and the results, so part of the second instruction steam must go there to be stored);

Storing a mapping table relating a plurality of triggers to respective ones of a plurality of different sequences of the non-essential code (Asghar figures 8 and 10, abstract, column 3 line 61-column 4 line 11);

Processing the essential code from the first memory in a microarchitecture structure until detecting an occurrence one of the triggers (Asghar figures 1 and 3, abstract, column 4 lines 11-67); and

Thereafter, processing one of the non-essential code sequences in the same microarchitecture structure, the one sequence being specified by the one trigger (Asghar figures 1 and 3, abstract, column 4 lines 11-67; in figure 1 both the GP CPU and the DSP are shown in the same CPU).

14. Referring to claim 34 Asghar has taught wherein the first and second memories are first and second pipelines (Asghar figure 4 abstract, column 4 lines 11-67).

15. Referring to claim 35 Asghar has taught wherein the first and second memories are caches (Asghar figure 4, numbers 444, 202)

16. Referring to claim 36 Asghar has taught wherein the first and second memories are logically separate (Asghar figure 4 abstract, column 4 lines 11-67).

17. Referring to claim 37 Asghar has taught wherein the first and second memories are physically separate (Asghar figures 1 and 4 abstract, column 4 lines 11-67).

18. Referring to claim 38 Asghar has taught wherein the non-essential code includes hint code (Asghar figure 4 abstract, column 4 lines 11-67; since the DSP replacement code will be performing instructions that aren't normally apart of the GP functions that are normally executed for the purpose of reducing the execution time, they would be "hints").

19. Referring to claim 39 Asghar has taught wherein the non-essential code includes sequences to perform one or more functions selected from the group consisting of

prefetching essential code into the first memory, testing the microarchitecture, security checking or sandboxing, speculative execution, interrupt or exception processing, and instruction set virtualization (Asghar figure 4 abstract, column 4 lines 11-67; the DSP performs instruction set virtualization by performing the same function as the GP instruction set, but using a DSP set to make it faster).

20. Referring to claim 40 Asghar has taught wherein the included sequences perform respectively multiple ones of the functions (Asghar figure 4 abstract, column 4 lines 11-67).

21. Referring to claim 41 Asghar has taught wherein certain of the essential code is stored in the second memory (Asghar figure 4, number 444, abstract, column 10 lines 45-64; the data cache holds the operands for the DSP functions and the results and the GP operands are stored there as well).

22. Referring to claim 42 Asghar has taught wherein the certain essential code includes sequences for virtualization (Asghar figure 4 abstract, column 4 lines 11-67; the DSP performs instruction set virtualization by performing the same function as the GP instruction set, but using a DSP set to make it faster).

23. Referring to claim 43 Asghar has taught wherein at least one of the sequences virtualizes one or more entities selected from the group consisting of:

individual instructions, blocks of instructions, sets of register, and processor hardware resources (Asghar figure 4 abstract, column 4 lines 11-67; the DSP performs instruction set virtualization by performing the same function as the GP instruction set, but using a DSP set to make it faster).

24. Referring to claim 44 Asghar has taught where the triggers are selected from the group consisting of one or more of instruction attributes, data attributes, state attributes, and event attributes (Asghar figures 8 and 10, abstract, column 3 line 61-column 4 line 11; the instruction attributes of the DSP functions).

25. Referring to claim 45 Asghar has taught where the instructions attributes include opcodes, locations, and/or operands (Asghar figures 8 and 10, abstract, column 3 line 61-column 4 line 11; the pattern recognition would recognize the opcodes).

26. Referring to claim 46 Asghar has taught wherein the data attributes include values and/or locations (Asghar figures 8 and 10, abstract, column 3 line 61-column 4 line 11).

27. Referring to claim 47 Asghar has taught wherein the state attributes include architectural and/or microarchitecutal states (Asghar figures 8 and 10, abstract, column 3 line 61-column 4 line 11).

28. Referring to claim 48 Asghar has taught wherein the event attributes include interrupts, exceptions, and/or processor state register values (Asghar figures 8 and 10, abstract, column 3 line 61-column 4 line 11).

29. Referring to claim 49 Asghar has taught a system comprising:

A processor including:

First and second pipelines for essential and non-essential code respectively (Asghar figure 1, numbers 102, 212, 214, abstract, column 4 lines 11-67; the code being executed by the DSP is not essential, and could be left unexecuted, and could just allow the CPU to execute as normal, but the code pattern is recognized and then executed optimally by the DSP portion of the processor)

A mapping table to relate a plurality of triggers to a plurality of sequences of the non-essential code (Asghar figures 8 and 10, abstract, column 3 line 61-column 4 line 11),

A microarchitecture structure coupled to the pipelines for processing the essential and to process the sequences in response to their respective triggers (Asghar figure 1, numbers 102, 212, 214, abstract, column 4 lines 11-67);

Memory coupled to the pipelines to store the essential and the non-essential code as separate parts of the same library (Asghar figure 4, number 444, abstract, column 10 lines 45-64; the data cache holds the operands for the DSP functions and the results and the GP operands are stored there as well; since a library is just a collection of items, the collections of the different operands, which are part of the instruction, for both the GP instructions and the DSP instructions reside in the cache).

30. Referring to claim 50 Asghar has taught wherein the memory includes at least one cache (Asghar figure 4).

31. Referring to claim 51 Asghar has taught wherein the memory includes one or more of a hard disk, a floppy disk, RAM, ROM, a flash memory, and/or a medium readable by a machine (Asghar figure 1).

32. Referring to claim 52 has taught where the memory stores the essential and non-essential code in separate sections of a file (Asghar figure 4, number 444, abstract, column 10 lines 45-64; since the file is not defined, each operand stored in the cache can be viewed as "file" which are stored separately).

33. Referring to claim 53 has taught where the essential and nonessential code reside in a static file (Asghar figure 4, number 444, abstract, column 10 lines 45-64).

34. Referring to claim 54 has taught where the nonessential code resides at least partly in a run-time library (Asghar figure 4, number 444, abstract, column 10 lines 45-64; the cache is updated in run-time).

Response to Arguments

35. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

36. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 09/24/03 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 609(B)(2)(i). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:30 P.M. with every other Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Charles Allen Harkness

Examiner

Art Unit 2183

March 4, 2004